A High Performance and Low DC Power V-band MMIC LNA Using 0.1 μm InGaAs/InAlAs/InP HEMT Technology

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Abstract—**We report the design and performance of state-of-the-art V- band MMIC LNA's using 0.1-μm gate length pseudomorphic $In_{0.60}Ga_{0.40}As/In_{0.52}Al_{0.48}As/InP$ HEMT's. The three-stage V-band LNA demonstrated an average of 3.0 dB noise figure between 56–64 GHz with 24–25.5 dB associated gain with a noise figure of 2.7 dB measured at 62 GHz. Furthermore, the dc power dissipation of this circuit was only 19.5 mW which is less than one-third the dc power dissipation of InGaAs/AlGaAs/GaAs HEMT versions. These results demonstrate the excellent potential of InP HEMT technology for millimeter-wave and low dc power applications.**

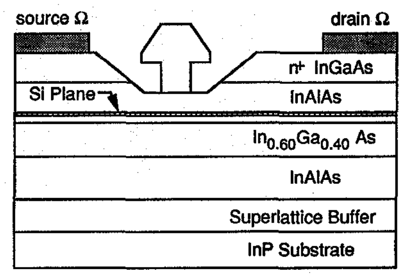

Fig. 1. Layer structure of an $In_{0.60}Ga_{0.40}As/In_{0.52}Al_{0.48}As/InP$ HEMT grown by MBE.

I. Introduction

V-BAND low noise amplifiers (LNA's) represent a critical component for many communications and weapon systems applications including satellite links, smart munitions, and phased arrays. The development of a monolithic V-band LNA as well as the monolithic integration of the LNA with other components will be important to lower cost, size, and weight and improved reliability and functionality compared to hybrid versions. Previously reported work include a four-stage GaAs-based HEMT V-band MMIC LNA which demonstrated 4–5 dB noise figure from 58–63 GHz with greater-than-22-dB associated gain for a four-stage V-band LNA [1] and a two-stage InP-based HEMT V-band MMIC LNA which demonstrated an average of 4.2 dB noise figure from 56–60 GHz with an average of 15.7 dB associated gain [2]. InP-based HEMT's have demonstrated the best gain and noise performance on a discrete device level at millimeter-wave frequencies [3]–[7]. The reasons include a high conduction band discontinuity at the InGaAs/InAlAs heterostructure interface, and the excellent electron mobility and peak velocity in the InGaAs channel. Increasing the indium mole fraction in the $In_xGa_{1-x}As$ ($x > 0.53$) channel enhances these advantages. We report here a state-of-the-art monolithic three-stage V-band LNA using 0.1-μm-gate-length pseudmorphic $In_{0.60}Ga_{0.40}As/In_{0.52}Al_{0.48}As/InP$ HEMT (PM InP HEMT) MMIC technology with low dc power dissipation. The first pass success for this design is primarily due to accurately generated active and passive models, a proven circuit design approach, greater process maturity, high quality material, and excellent device performance.

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II. Device Design

The PM InP HEMT structure (shown in Fig. 1) is grown using molecular beam epitaxy on a two-inch InP substrate. Silicon planar doping is employed in the InAlAs layer to simultaneously achieve a high channel aspect ratio for a 0.1-μm-gate-length device and high electron transfer efficiency. Typical room temperature and 77K Hall mobilities are 10 500 and 35 000 respectively with a sheet carrier concentration of 3.0×10^12 cm^-2. The design is further optimized for good pinchoff characteristics and high transconductance. Other design considerations include a thick highly doped InGaAs cap layer and an optimized device layout to minimize parasitic capacitances and resistances.

The 0.1-μm-gate-length PM InP HEMT has achieved transconductances, G_m, greater than 1300 mS/mm, cutoff frequencies, f_T, of 240 GHz, and maximum oscillation frequencies, f_{max}, of 400 GHz at a drain bias of 1 V. The devices are typically designed and fabricated to have a gate voltage for peak G_m between 0.0 and +0.1V. A measured noise figure of 1.3 dB at 95 GHz with an associated gain of 8.2 dB [3], and a measured gain of 7.3 dB at 140 GHz [4] were obtained from single-stage hybrid amplifiers using these devices. The PM InP HEMT was used for the construction of a state-of-art three-stage wide-band 60–75 GHz hybrid cryogenically-cooled amplifier demonstrating a noise figure of 0.6–0.8 dB and 14–16 dB associated gain[5].

III. Amplifier Design and Fabrication

The linear small signal model for a 0.1-μm-gate-length four finger, 40-μm-gate-width PM InP HEMT used for the three-stage V-band LNA was derived from carefully fitting to the measured small signal S-parameters from 1 to 40 GHz [3], [9],

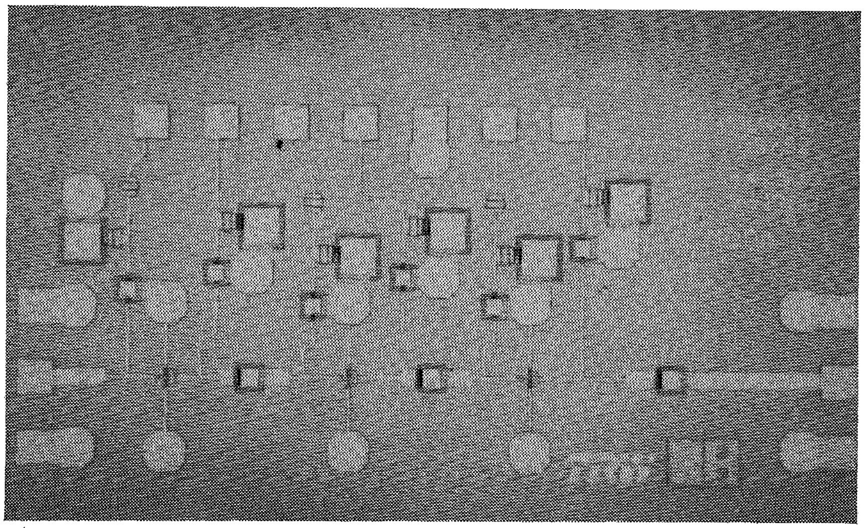

Fig. 2. Photograph of the 3-stage PM InP HEMT MMIC V-band LNA with a total chip size of 3.35 × 2.0 mm^2.

[10]. The noise model parameters are obtained from fitting measured noise parameters from 2 to 26 GHz. The devices are biased at a drain voltage of 0.8 volts and at various gate biases. At 60 GHz, the modeled device noise parameters are $\Gamma opt = 0.487 < 50.6°$ and R_n = 41 ohms.

The three-stage V-band LNA uses a single-ended design with each stage consisting of a 40-μm-gate-width PM InP HEMT. The input and interstage matching networks were designed for low noise figure and were constructed using cascading high–low impedance microstrip lines. NiCr TFR, radial stubs, and MIM capacitors were used for the biasing networks. The circuit was also carefully designed to ensure amplifier stability.

The InP HEMT MMIC fabrication process was derived from the baseline GaAs-based HEMT MMIC production process [8]. This approach helped improve the chance of first pass success for the V-band LNA circuit. Key differences are the isolation and ohmic contact process, and gate process. NiCr thin film resistors (TFR) with 100 ohm/sq. nominal resistance were used, and metal-insulator-metal capacitors were formed using silicon dioxide as the dielectric yielding a capacitance of 125 pF/mm^2. The InP substrate was thinned and backside via holes were etched for circuit grounding.

IV. Amplifier Results

A picture of the monolithic V-band LNA with a total chip size of 3.35 × 2.0 mm^2 is shown in Fig. 2. The noise and gain of the amplifier were measured on-wafer by Cascade Microtech RF probes. The amplifier demonstrated an average noise figure of 3 dB from 56–64 GHz with 24–25.5 dB associated gain from 56–64 GHz as shown in Fig. 3. At 62 GHz, the noise figure was measure to be 2.7 dB. This performance is the best ever reported to our knowledge for monolithic LNA's in this frequency range. Compared to GaAs-based HEMT V-band LNA results and previous InP HEMT V-band LNA results [1], [2], this LNA demonstrates an improvement of greater than 1 dB in overall noise figure and 1–2 dB in gain per stage. Also, the overall dc power dissipation of the circuit was 19.5 mW ($V_d = 0.75V, I_{dtotal} = 26$ mA) which is more than 3 times less than the GaAs version. Low dc power consumption is very important in both portable systems and phased arrays where lower power dissipation is necessary. The low dc power dissipation of the PM InP HEMT is due mainly to the high electron mobility of the InGaAs channel which results in a low drain saturation voltage and lower applied drain bias and excellent device pinchoff characteristics which results in a minimum device noise figure at lower drain currents.

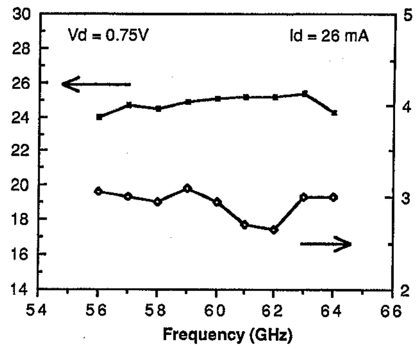

Fig. 3. Measured noise figure and gain characteristics for the 3-stage PM InP HEMT MMIC V-band LNA biased at $V_d = 0.75$V and $I_d = 24$ mA.

V. Conclusion

We have demonstrated a state-of-the-art 0.1-μm-gate-length PM InP HEMT V-band MMIC three-stage LNA with an average of 3 dB noise figure and 24–25.5 dB associated gain from 56–64 GHz. The circuit also demonstrated ultra-low dc power dissipation of 19.5 mW. This result demonstrates the potential for insertion of InP HEMT MMIC technology into various millimeter-wave systems with the advantages of superior performance, lower cost, lower weight, and multifunction capability.

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